

REMARKS

Claims 4, 7, 9-20 and 22-24 remain in the application. This is the sixth Office Action by the USPTO in this case. Applicants have had the following prior rejections, including three Final Rejections:

1. Puchner et al. U.S. Patent 6,156,620 and Puntambekar et al. U.S. Patent No. 5,714,037 were cited against Applicants' claims 1-23 in the First Office Action mailed June 5, 2001;
2. Puntambekar et al. U.S. Patent No. 5,714,037 was cited against Applicants' claims 1-23 in the First Final Rejection mailed July 31, 2002;
3. Puntambekar et al. U.S. Patent No. 5,714,037 was again cited against Applicants' claims 4-24 in the Second Final Rejection (Third Office Action) mailed October 24, 2002;
4. Puntambekar et al. U.S. Patent No. 5,714,037 and Barnes et al. U.S. Patent 5,284,549 were cited against Applicants' claims 4-24 in the Fourth Office Action mailed January 7, 2003; and
5. Li et al. U.S. Patent 6,284,149 and Kadomura U.S. Patent 5,266,157 were cited against Applicants' claims 4-7 and 9-19, and 21-24; and the Li patent, the Kadomura patent, and Guinn et al. U.S. Patent 5,877,032 were cited against Applicants' claim 20 in the Third Final Rejection (Fifth Office Action) mailed June 4, 2003.

I. **SUMMARY OF THE OCTOBER 22ND, 2003 OFFICE ACTION**

Section 103 Rejections

Claims 4, 7, and 9-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McInerney et al. U.S. Patent 4,690,746 in view of Cohen et al. U.S. Patent 6,346,489.

Claims 19-20 and 22-24 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over the McInerney et al. patent in view of the Cohen et al. patent.

II. **THE REFERENCES**

A. **The McInerney et al. Reference**

McInerney et al. U.S. Patent 4,690,746 teaches a method for producing a film over a topologically non-planar surface of a material which has a sputter etch rate which is higher in a direction parallel to the plane of the wafer than in a direction perpendicular to the plane of the wafer. Key steps in the process include first, depositing the material by plasma enhanced chemical vapor deposition while simultaneously sputter etching it. Then, in a second step, the material is sputter etched alone. Using this two step process, a substantially conformal or sloped film is produced by repeating the steps consecutively until the desired thickness is obtained. The film can then be substantially planarized if desired, by an extended sputter etch to selectively remove material having a sloped surface rather than a flat surface, since the etch rate is higher parallel to the plane of the wafer than perpendicular to the wafer. If a thicker planar surface is desired, additional material can then be deposited by steps of

simultaneous plasma chemical vapor deposition and sputter etch, or by consecutive steps of simultaneous plasma deposition and sputter etch followed by sputter etching.

B. The Cohen et al. Reference

Cohen et al. U.S. Patent 6,346,489 discloses a precleaning process suitable for fabricating metal plugs in a low-k, carbon-containing dielectric. More specifically, the invention is a process for cleaning a contact area of a metal conductor on a semiconductor workpiece so as to remove native oxide while minimizing damage to a low-k, carbon-containing dielectric overlying the metal. After forming contact openings in the low-k dielectric so as to expose contact areas on the underlying metal conductor, the contact areas are cleaned by exposing the workpiece to an atmosphere formed by plasma decomposition of a mixture of hydrogen-containing and helium gases. The preclean process is said to be capable of repairing damage to the dielectric caused by preceding process steps, such as oxygen plasma ashing processes for removing photoresist.

III. THE INVENTION

The invention comprises a process for etching oxide wherein a reproducibly accurate and uniform amount of silicon oxide can be removed from a surface of an oxide layer previously formed over a semiconductor substrate. The oxide is exposed, in an etch chamber, to a plasma consisting essentially of a nitrogen plasma generated by a first rf power source which is maintained at a power level ranging from about 250 watts to about 1000 watts. At the same time, an rf bias, generated by a second rf power supply maintained at a power level of from above zero up to a power level just below a level at which sputtering of said substrate materials would commence, is applied to the substrate support on which the substrate is

Appl. No. 09/464,297
Amendment dated January 22, 2004
Reply to Office Action of October 22, 2003

Docket No. 99-039/RCE

supported in the etch chamber. The thickness of the oxide removed in a given period of time may be changed by changing the amount of rf bias applied to the substrate by the second rf power source through the substrate support.

IV. **DISCUSSION**

All of the claims (4, 7, 9-20 and 22-24) were rejected under 35 U.S.C. § 103(a) as being unpatentable over McInerney et al. U.S. Patent 4,690,746 in view of Cohen et al. U.S. Patent 6,346,489.

A. **The McInerney et al. Reference**

The Office Action states that: "McInerney et al. disclose a process for *etching a fixed thickness* of silicon dioxide/oxide from a silicon dioxide/oxide layer formed on a semiconductor substrate in a process chamber 15/etching apparatus." (emphasis added)

First of all, McInerney et al. disclose a deposition and planarization process, not an etching process. While they do disclose carrying out deposition and etching in the same step followed at least optionally with a second etching step, the net operation of their process is a deposition of additional material, not a reduction. The patentees refer to this in Figure 6a and the accompanying text at column 4, lines 26-48. The patentees further explain this in column 3, lines 49-52, where they state:

"The plasma enhanced CVD of dielectric material and the sputter etching away for the deposited material occur at the same time but with *a net accumulation*." (emphasis added)

Thus, the McInerney et al. process is a deposition process, not an etching process wherein less material (not more) remains after the process. One skilled in the art, seeking to carry out an etching or material removal process, would not look to a deposition process for instruction.

With respect to the alleged removal of a *fixed thickness* of silicon dioxide/oxide during the etching step or steps of the McInerney et al. deposition process, Applicants have not been able to locate such teachings in the McInerney et al. reference. Identification of the location of this teaching is hereby requested. (The same may be said for the term *dioxide/oxide*.) If the McInerney et al. patent teaches anything regarding thickness, it is believed to be that the deposited material etches at different rates, depending on the angle of the surface of the deposited material. In column 2, lines 8-11, McInerney et al. state:

"The film can then be substantially planarized if desired, by an extended sputter etch, since the etch rate is **higher parallel to the plane of the wafer than perpendicular to the wafer.**" (emphasis added)

If their etch rate varies across their wafer, the McInerney et al. etch step in their deposition process, cannot remove a *fixed thickness* of dioxide/oxide from their substrate.

The Rejection goes on to state that the McInerney et al. oxide surface is exposed to a plasma generated by a gas mixture of N₂O, argon, and silane (SiH₄), and then says that this reads on exposing the oxide surface to a plasma consisting essentially of a nitrogen plasma. Applicants take issue with this statement. One skilled in the art knows that plasmas generated by different gases and mixtures of gasses have different properties and therefore behave differently. Nothing has been found in McInerney et al. which would suggest that a plasma generated by a gas mixture of N₂O, argon, and silane (SiH₄) will have the same properties as a nitrogen plasma, and no passage in the McInerney et al. patent supporting such a contention has been furnished.

The McInerney et al. patent then teaches the use of a self-induced DC bias, apparently to permit use of a potential below ground. The Rejection states that McInerney et al. differs from the claimed invention by maintaining a DC bias from an rf source instead of an rf bias. Applicants must note here that McInerney et al. refer to a DC blocking capacitor and a matching network as the source of their DC bias on their electrode, not an rf source. Furthermore, this is by no means inclusive of all of the differences between Applicants' claimed invention and the teachings of McInerney et al.

All of Applicants' independent claims (4, 11, 19, & 24) refer to the use of an *rf* bias from a second rf power source to provide an rf bias to their electrode. McInerney et al. have no such second rf power source - nor do they apparently need such a second rf power source since they do not use an rf bias, but rather self-induce a DC bias using a DC blocking capacitor and a matching network. They say that this use of a DC bias enables them to negatively bias their substrate (turret electrode) to a below ground potential.

Most importantly, Applicants' teach and claim the use of this rf bias to the substrate in their apparatus to accurately control the thickness or amount of oxide removed from the oxide layer during their plasma etch. An increase in rf bias, in turn, results in an increase in the amount of oxide removed. This was quite surprising in view of the relative insensitivity of the process to changes in the rf power level of the first rf power supply.

In summary, then, Applicants claim an etching process which uses *a nitrogen plasma* in combination with *an rf bias* from *a second rf power supply* and coupled to the substrate *to control* the amount of material removed. McInerney et al. disclose an deposition process which uses a DC bias in combination with a plasma formed from a gas mixture of N₂O,

argon, and silane (SiH_4) to provide a more planarized deposition. The teachings of the McInerney et al. patent do not suggest Applicants' process.

B. The Combination of McInerney et al. and Cohen et al.

The USPTO, after commenting on the shortcomings of the McInerney et al. patent (last two lines of page three of the Office Action), further states that Cohen et al., in a method of precleaning that minimizes damage to an underlying low k dielectric layer, discloses that a bias rf power supply can help ignite and sustain the plasma and can produce a DC bias voltage on the pedestal.

Cohen et al. U.S. Patent 6,346,489 teaches the removal of native oxide from exposed metal surfaces beneath patterned photoresist and dielectric layers using a hydrogen-containing plasma. Cohen et al., at column 4, lines 45-46, states that, "The hydrogen-containing plasma is maintained as long as necessary to remove the native oxide...". Cohen et al. states that a bias rf power supply connected to the pedestal can help *ignite* and *sustain* the plasma. However, Cohen et al. **teach or suggest nothing** with regard to the use of an adjustable rf power source to *control* the thickness of the oxide removed. Rather, it is their desire to remove *all* of their native oxide. From the remarks of Cohen et al., at column 3, line 57 to page 4, line 27, concerning the function and utility of such an rf bias power source, one skilled in the art might infer that such a second rf power source is a tolerated nuisance, but certainly not that such a second rf power source can be used to control the amount of native oxide removed. Cohen et al. state (at column 3, line 57 to column 4, line 27):

"A second rf power supply 38, also called a bias RF power supply, supplies F power to the pedestal. The bias RF power supply *can help guide and sustain the plasma*, and it can produce a DC bias voltage on the pedestal that in most cases is negative relative to the plasma body. The negative bias voltage accelerates ions from the plasma toward the susceptor." (emphasis added)

"Since RF bias power *increases the risk of damage to the dielectric by ion bombardment*, we prefer using *the lowest possible RF bias power*. We believe *we can successfully remove native oxide from the metal 12 without any RF bias power applied to the pedestal*. However, in the illustrated inductively-coupled plasma chamber, some RF bias power usually is required to initiate or "strike" the plasma. In addition, a small amount of RF power can ensure that changing process conditions do not extinguish the plasma. Therefore, in our preferred implementation embodiment, we program the controller 44 to command the bias RF power supply 38 to initially apply to the pedestal 40 watts of RF power at a frequency of 13.56 MHz in order to initiate or strike the plasma, and to then reduce the bias rf power to 10 watts *throughout the precleaning process*. At low power levels such as the preferred 10 watts, we find the DC bias voltage *is close to zero*, and even can be positive in the preferred chamber of FIG. 3."

"In a chamber having a remote plasma source, we do not believe there would be any need to apply RF bias power to the pedestal." (emphasis added)

Thus, it is obvious that Cohen et al. contains no suggestion to use an RF bias power as a second RF power source to control the thickness or amount of oxide removed during the process. There is, therefore, no suggestion in Cohen et al. of the desirability of combining the two references in a manner which would suggest Applicants' claimed process.

The CAFC, and its predecessor court, the CCPA, have long held that a reference must contain something to suggest desirability of combining references. In the case of *In re Imperato* 179 USPQ 730, the CCPA stated, at page 732:

"With regard to the principle rejection, we agree that combining the teaching of Schaefer with that of Johnson or Amberg would give the beneficial result observed by appellant. However, the mere fact that these disclosures *can* be combined does not make the combination obvious unless the art also contains something to suggest the desirability of the combination." (Emphasis in original text)

In the case of *In re Regal, Buchel and Plempel*, 188 USPQ 136 (1975), the CCPA stated on page 139:

"...there must be some logical reason, apparent from positive, concrete evidence of record which justifies a combination of primary and secondary references...Further, as we stated in *re Bergel*...130 USPQ 206, 208 (1961): The mere fact that it is *possible* to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." (emphasis in original)

The Court of Appeals for the Federal Circuit (CAFC) has continued to require that there be such a suggestion of desirability of such combinations and/or such modifications in references being cited. (*C. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221

USPQ 481, Fed. Cir., 1984; ACS Hospital Systems, Inc. v. Montefiore Hospital et al, 221 USPQ 929, Fed. Cir., 1984; In re Gordon, 221 USPQ 1125, Fed. Cir., 1984; and In re Grabiak, 226 USPQ 870, Fed. Cir., 1985.)

In Lindemann, the Court stated, at page 488:

"The claimed invention must be considered as a whole, and the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination."

The court then cited, with approval, In re Imperato, 179 USPQ 730, and In re Sernaker, 217 USPQ 1.

In the ACS Hospital Systems case, the CAFC stated, at page 933:

"Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined *only* if there is some suggestion or incentive to do so. The prior art of record fails to provide any such suggestion or incentive." (emphasis in original)

The ACS Hospital Systems case was later cited with approval in the case of In re Geiger, 2 USPQ 2d 1276, Fed. Cir., 1987, at page 1278.

In the case of In re Gordon, the CAFC stated, at page 1127:

"The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."

In the Case of In re Grabiak, the CAFC, at page 872, repeated the statement in the CCPA case of In re Bergel (130 USPQ 206), that:

"The mere fact that it is *possible* to find two isolated disclosures which might be combined in such a way to produce a new compound does not necessarily render such production obvious unless the art also contains something to suggest the desirability of the proposed combination." (Emphasis in original)

More recently the CAFC stated, in the case of In re Newell, 13 USPQ 2d 1248 (1989), at page 1250:

"..a retrospective view of inherency is not a substitute for some teaching or suggestion which supports the selection and use of the various elements in the particular claimed combination."

In the case of In re Rouffert, 47 USPQ 2d 1453 Fed. Cir., 1998, the CAFC stated, at page 1456:

"When a rejection depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references."

citing with approval In re Geiger, 2 USPQ 2d 1276, Fed. Cir., 1987, at page 1278.

The cited references, McInerney et al. and Cohen et al., do not contain the required suggestions for the desirability of combining them together in a manner which would render Applicants' process obvious. Neither McInerney et al. nor Cohen et al. contain any teachings regarding the use of a second RF power source coupled to the pedestal to control the amount of oxide removed; McInerney et al. teaches the use of DC bias power to sputter etch while depositing; and Cohen et al. teaches that a secondary RF power, if used at all, is used to strike the plasma, after which is lowered to a minimum power level (10 watts) and maintained

at this low power level throughout the Cohen et al. precleaning process. Applicants' claimed process is patentable over this cited combination of references.

C. **The Priority of Applicants' Invention over Cohen et al.**

Cohen et al. U.S. Patent 6,346,489 has a priority date (filing date) of September 2, 1999. The enclosed affidavit under Rule 131 establishes a conception date by Applicants prior to the September 2, 1999 filing date of Cohen et al. Exhibits C1-C3 of the accompanying Rule 131 declaration serves to function not only as evidence of conception prior to the September 2, 1999 Cohen et al. filing date, but further arguably functions as evidence of an actual reduction to practice prior to the September 2, 1999 Cohen et al. filing date. The affidavit establishes diligence commencing prior to the Cohen et al. September 2, 1999 filing date and extending to Applicants' December 15, 1999 filing date. The affidavit further establishes that Applicants' patent application was filed within a reasonable time after the reduction to practice of the invention, as required by the courts when actual reduction to practice has been established prior to the critical date, but the filing date of the first to reduce to practice is after the critical date.

With respect to the required "reasonable time period" between the actual reduction to practice and the subsequent filing date, the courts have held that this will vary from case to case. *Young v. Dworkin*, 180 USPQ 388, at page 391. However, it should be noted that the reduction to practice in this case occurred on February 5, 1999 and the filing date was December 15, 1999, i.e., less than 10½ months later. No cases were found in which a filing date of less than a year after actual reduction to practice was considered to be unreasonable.

Appl. No. 09/464,297
Amendment dated January 22, 2004
Reply to Office Action of October 22, 2003

Docket No. 99-039/RCE

If the Examiner in charge of this case feels that there are any remaining unresolved issues in this case, the Examiner is urged to call the undersigned attorney at the below listed telephone number which is in the Pacific Coast Time Zone.

Respectfully Submitted,


John P. Taylor, No. 22,369
Attorney for Applicants
Telephone No. (909) 303-1416

Mailing Address:

Sandeep Jaggi, Chief Intellectual Property Counsel
LSI Logic Corporation
Legal Department - IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035